

REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Claims 13-22 and 26-25 are pending in the application. Claims 13 and 26 are independent.

The undersigned and Mr. Omar Nassif would like to thank Examiner Warren for the cordial and productive interview of December 13, 2005. The Examiner's helpful comments and suggestions were instrumental in preparing this response.

As discussed at the interview, Applicant has amended claim 13 and added new claims 26-32 to afford a scope of protection commensurate with the disclosure. The amended claim as well as the new claims are fully supported in the specification and drawings, and are believed to be allowable. Specifically, support can be found in the specification in paragraphs 55 and 56 (of the application as published) and are further illustrated in Figure 10. Accordingly, no new matter has been added as a result of this amendment.

Also, as discussed during the interview, Applicant resubmits herewith a copy of the Information Disclosure Statement (IDS) previously submitted by Applicant's previous agents. The IDS was submitted June 28, 2005 and cited prior art uncovered during the search in Applicant's corresponding Patent Cooperation Treaty (PCT) application. According to PAIR, the IDS was assigned a mail room date of July 1, 2005.

The Examiner had rejected claims 1-25 pending in the application. Specifically, claims 1-5, 8-10, 12-17, 23, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani (US 6,120,301) in view of Kimura (US 5,396,104). Claims 6, 7 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani in view of Kimura and Ball (US Pub 2002/0045290 A1). Claims 18-20 and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani in view of Kimura and Bockelman et al. (US 5,471,010). Claims 21 and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ichitani in view of Kimura and Murdoch (US 4,002,282).

Applicant has deleted claims 1-12 and 23-25 with traverse in order to expedite prosecution of the application and reserves the right to pursue these claims in a continuing application.

Accordingly, the rejection of these claims are moot. Further, Applicant respectfully traverses the rejection to claims 13-22.

As discussed in the interview, independent Claim 13 recites an novel integrated circuit package comprising: a substrate devoid of horizontal traces, said substrate having terminal pads arranged along a perimeter of a surface of said substrate; electrically conductive vias connecting said terminal pads directly to connectors aligned with the terminal pads on an opposite side of said substrate; a semiconductor chip mounted on the substrate, inside said perimeter, said chip having bond pads located on a surface of said chip; and a plurality of insulated bond wires, each of said bond wires extending from a bond pad on said chip to a terminal pad on said substrate.

As discussed at the interview, neither Ichitani nor Kimura, nor a combination thereof, teach or suggest an integrated circuit package as defined in claim 13. Specifically, Kimura teaches nothing more than the use of insulated bonding wire.

Ichitani relates to manufacturing a Ball Grid Array (BGA) semiconductor device, wherein the a surface of the substrate is supported by being bonded to a frame. In the description, Ichitani teaches a substrate having terminal pads (12) and connectors (13). Additionally, in column 5, lines 29-37, Ichitani teaches that the upper terminals 12 and lower terminals 13 are connected via wires 14, not vias. Further, Ichitani goes on to teach that the wires are "electrically insulated from each other" and are "patterned in each of the layers in the base formed in a multilayer structure".

Accordingly, as discussed at the interview, Applicant submits that Ichitani does not teach a substrate devoid of horizontal traces. This is illustrated by the fact that every drawing, the wire between a connector and a terminal pad includes a jog. Further, as illustrated in Figure 4(a), 5(a), 9(a) and 11(a) of Ichitani, the connectors are not aligned with the terminal pads on the substrate. In fact, Ichitani teaches away from aligning connectors and terminal pads by stating that the BGA has "external terminals disposed on the *entire main surface* of the package enabling the number of pins to be increased without increasing the size of the package" (column 1, lines 20-23).

Also, as discussed at the interview, the references filed as part of the IDS submitted herewith do

not include the elements defined in Claim 13.

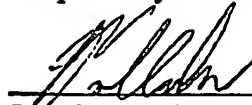
Yet further, as also discussed at the interview, independent claim 26 recites a novel integrated circuit package comprising a substrate element having first and second opposed surfaces. A plurality of terminal pads are disposed on a peripheral portion of the first opposed surface and a plurality of connectors are disposed on a peripheral portion of the second opposed surface to define an array of pairs. Each pair comprises a terminal pad and a connector in alignment with one another, and an electrically conducting via interconnecting the terminal pad to the connector, the electrically conducting via comprising a pair of straight walls interconnecting the first and second opposed surfaces. A semiconductor chip is mounted in a central portion of the first opposed surface, the semiconductor chip comprising a plurality of bond pads on a surface thereof. Bond wires interconnect bond pads on the semiconductor chip to terminal pads on the substrate element.

For reasons similar to those described above as discussed at the interview, Applicant submits that independent claim 26 is neither taught nor suggested by the prior art.

In view of the above, it is believed that this application is now in condition for allowance, and a Notice thereof is requested.

If the Examiner has further concerns, he is encouraged to contact Applicant's undersigned agent.

Respectfully submitted,



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